

Battery Management Unit Impedance Track™ Fuel Gauge for Use With the bq2419x Charger Controller

Check for Samples: [bq27531-G1](#)

FEATURES

- **Battery Fuel Gauge and Charger Controller for 1-Series Li-Ion Applications**
- **Resides on System Main Board**
- **Battery Fuel Gauge Based on Patented Impedance Track™ Technology**
 - Models the Battery Discharge Curve for Accurate Time-to-Empty Predictions
 - Automatically Adjusts for Battery Aging, Battery Self-Discharge, and Temperature/Rate Inefficiencies
 - Low-Value Sense Resistor (5 mΩ to 20 mΩ)
- **Battery Charger Controller with customizable charge profiles**
 - Configurable Charge Voltage and Current based on Temperature
 - Optional State of Health (SoH) and Multi-level based charge profiles
- **Host Free Autonomous Battery Management System**
 - Reduced software overhead allows for easy portability across platforms and shorter OEM design cycles
 - Higher safety and security
- **Run Time Improvements**
 - Longer battery runtime leveraging Impedance Track technology
 - Tighter accuracy controls for charger termination
 - Improved recharged thresholds
- **Intelligent Charging - Customized and adaptive charging profiles**
 - Charger Control based on SoH
 - Temperature Level Charging (TLC)
- **Battery Charger Controller for bq2419x Single Cell Switchmode Battery Charger**
 - Stand-Alone Charging Solution
 - Ship mode capability
- **400-kHz I²C™ Interface for Connection to System Microcontroller Port**
- **In a 15-Pin NanoFree™ (CSP) Packaging**

APPLICATIONS

- **Smartphones, Feature phones and Tablets**
- **Digital Still and Video Cameras**
- **Handheld Terminals**
- **MP3 or Multimedia Players**

DESCRIPTION

The Texas Instruments bq27531-G1 system-side Li-Ion Battery Management Unit is a microcontroller peripheral that provides Impedance Track™ fuel gauging and charging control for single-cell Li-Ion battery packs. The device requires little system microcontroller firmware development. Together with bq2419x Single Cell Switchmode Charger, the bq27531-G1 manages an embedded battery (non-removable) or a removable battery pack.

The bq27531-G1 uses the patented Impedance Track™ algorithm for fuel gauging, and provides information such as remaining battery capacity (mAh), state-of-charge (%), run-time to empty (min), battery voltage (mV), temperature (°C) and state of health (%).

Battery fuel gauging with the bq27531-G1 requires only PACK+ (P+), PACK– (P–), and Thermistor (T) connections to a removable battery pack or embedded battery circuit. The CSP option is a 15-ball package in the dimensions of 2,61 mm × 1,96 mm with 0,5 mm lead pitch. It is ideal for space constrained applications.



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bq27531-G1

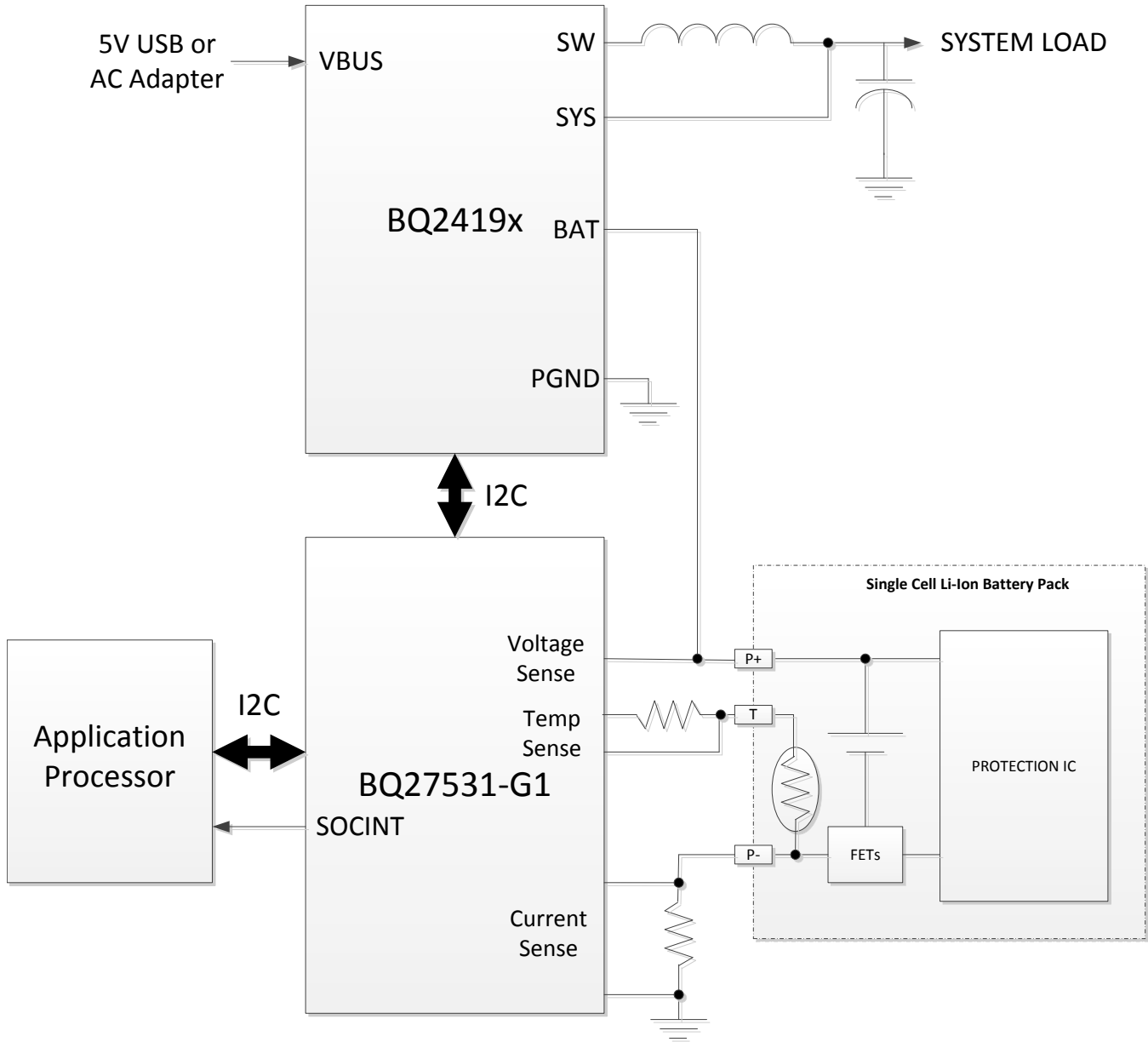
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TYPICAL APPLICATION



DEVICE INFORMATION

AVAILABLE OPTIONS

| PART NUMBER | FIRMWARE VERSION | PACKAGE | T _A | COMMUNICATION FORMAT | TAPE and REEL QUANTITY |
|----------------|------------------|---------|----------------|----------------------|------------------------|
| bq27531YZFR-G1 | 1.02 (0x0102) | CSP-15 | -40°C to 85°C | I ² C | 3000 |
| bq27531YZFT-G1 | | | | | 250 |

THERMAL INFORMATION

| THERMAL METRIC ⁽¹⁾ | | bq27531-G1 | UNITS |
|-------------------------------|--|---------------|-------|
| | | YZF (15 PINS) | |
| θ_{JA} | Junction-to-ambient thermal resistance | 70 | °C/W |
| $\theta_{JC(top)}$ | Junction-to-case(top) thermal resistance | 17 | |
| θ_{JB} | Junction-to-board thermal resistance | 20 | |
| ψ_{JT} | Junction-to-top characterization parameter | 1 | |
| ψ_{JB} | Junction-to-board characterization parameter | 18 | |
| $\theta_{JC(bottom)}$ | Junction-to-case(bottom) thermal resistance | n/a | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

PIN ASSIGNMENT AND PACKAGE DIMENSIONS

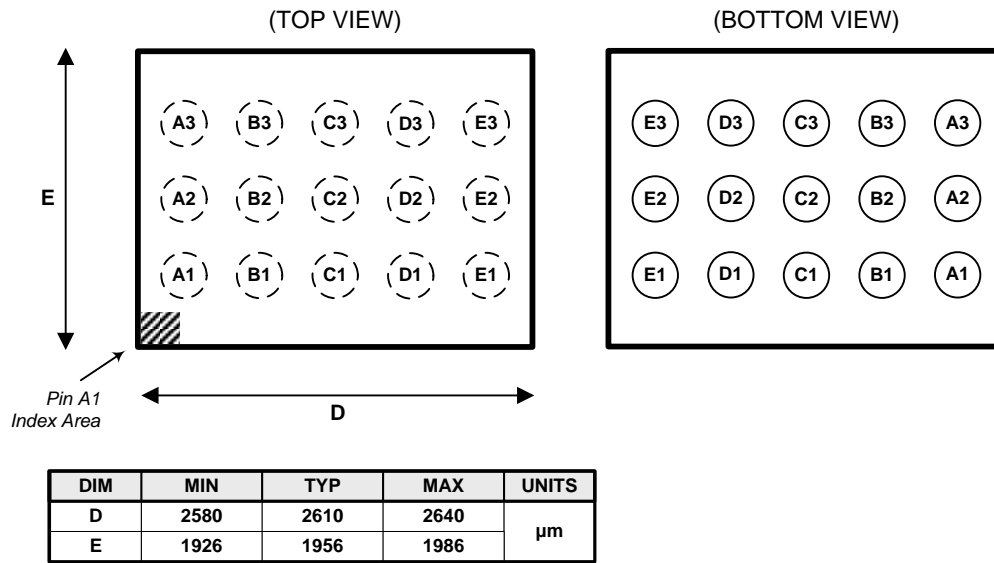


Table 1. PIN FUNCTIONS

| PIN | | TYPE | DESCRIPTION |
|---------|--------|------|--|
| NAME | NO. | | |
| SRP | A1 | IA | Analog input pin connected to the internal coulomb counter where SRP is nearest the PACK– connection. Connect to 5-mΩ to 20-mΩ sense resistor. |
| SRN | B1 | IA | Analog input pin connected to the internal coulomb counter where SRN is nearest the Vss connection. Connect to 5-mΩ to 20-mΩ sense resistor. |
| Vss | C1, C2 | P | Device ground |
| Vcc | D1 | P | Regulator output and bq27531-G1 power. Decouple with 1μF ceramic capacitor to Vss. |
| REGIN | E1 | P | Regulator input. Decouple with 0.1μF ceramic capacitor to Vss. |
| SOC_INT | A2 | I/O | SOC state interrupts output. Generates a pulse as described in bq27531-G1 Technical Reference Manual . Open drain output. |
| BSCL | B2 | O | Battery Charger clock output line for chipset communication. Push-pull output. |
| CE | D2 | I | Chip Enable. Internal LDO is disconnected from REGIN when driven low. Note: CE has an internal ESD protection diode connected to REGIN. Recommend maintaining $V_{CE} \leq V_{REGIN}$ under all conditions. |
| BAT | E2 | I | Cell-voltage measurement input. ADC input. Recommend 4.8V maximum for conversion accuracy. |
| SCL | A3 | I | Slave I ² C serial communications clock input line for communication with system (Master). Open-drain I/O. Use with 10kΩ pull-up resistor (typical). |
| SDA | B3 | I/O | Slave I ² C serial communications data line for communication with system (Master). Open-drain I/O. Use with 10kΩ pull-up resistor (typical). |
| BSDA | C3 | I/O | Battery Charger data line for chipset communication. Push-pull output. |
| TS | D3 | IA | Pack thermistor voltage sense (use 103AT-type thermistor). ADC input. |
| BI/TOUT | E3 | I/O | Battery-insertion detection input. Power pin for pack thermistor network. Thermistor-multiplexer control pin. Use with pull-up resistor >1MΩ (1.8 MΩ typical). |

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| PARAMETER | | VALUE | UNIT |
|--------------------|---|----------------------------------|------|
| V _{REGIN} | Regulator input range | -0.3 to 5.5 | V |
| | | -0.3 to 6.0 ⁽²⁾ | V |
| V _{CE} | CE input pin | -0.3 to V _{REGIN} + 0.3 | V |
| V _{CC} | Supply voltage range | -0.3 to 2.75 | V |
| V _{IOD} | Open-drain I/O pins (SDA, SCL, SOC_INT) | -0.3 to 5.5 | V |
| V _{BAT} | BAT input pin | -0.3 to 5.5 | V |
| | | -0.3 to 6.0 ⁽²⁾ | V |
| V _I | Input voltage range to all other pins (BI/TOUT, TS, SRP, SRN, BSDA, BSCL) | -0.3 to V _{CC} + 0.3 | V |
| ESD | Human-body model (HBM), BAT pin | 1.5 | kV |
| | Human-body model (HBM), all other pins | 2 | |
| T _A | Operating free-air temperature range | -40 to 85 | °C |
| T _{stg} | Storage temperature range | -65 to 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Condition not to exceed 100 hours at 25 °C lifetime.

RECOMMENDED OPERATING CONDITIONS

T_A = -40°C to 85°C, V_{REGIN} = V_{BAT} = 3.6V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|--|--|------|-----|-----|------|
| V _{REGIN} | Supply voltage | No operating restrictions | 2.8 | | 4.5 | V |
| | | No FLASH writes | 2.45 | | 2.8 | |
| C _{REGIN} | External input capacitor for internal LDO between REGIN and V _{SS} | Nominal capacitor values specified. Recommend a 5% ceramic X5R type capacitor located close to the device. | | 0.1 | | μF |
| C _{LDO25} | External output capacitor for internal LDO between V _{CC} and V _{SS} | | 0.47 | 1 | | μF |
| t _{PUCD} | Power-up communication delay | | | 250 | | ms |

SUPPLY CURRENT

T_A = 25°C and V_{REGIN} = V_{BAT} = 3.6V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|----------------------------------|---|-----|-----|-----|------|
| I _{CC} ⁽¹⁾ | Normal operating-mode current | Fuel gauge in NORMAL mode. I _{LOAD} > Sleep Current | | 118 | | μA |
| I _{SLP+} ⁽¹⁾ | Sleep+ operating mode current | Fuel gauge in SLEEP+ mode. I _{LOAD} < Sleep Current | | 62 | | μA |
| I _{SLP} ⁽¹⁾ | Low-power storage-mode current | Fuel gauge in SLEEP mode. I _{LOAD} < Sleep Current | | 23 | | μA |
| I _{HIB} ⁽¹⁾ | Hibernate operating-mode current | Fuel gauge in HIBERNATE mode. I _{LOAD} < Hibernate Current | | 8 | | μA |

- (1) Specified by design. Not production tested.

DIGITAL INPUT AND OUTPUT DC CHARACTERISTICS

 $T_A = -40^{\circ}\text{C}$ to 85°C , typical values at $T_A = 25^{\circ}\text{C}$ and $V_{\text{REGIN}} = 3.6\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|---|---|-----------------------|-----------------------|-----|---------------|
| V_{OL} | Output voltage, low (SCL, SDA, SOC_INT, BSDA, BSCL) | $I_{\text{OL}} = 3\text{ mA}$ | | | 0.4 | V |
| $V_{\text{OH(PP)}}$ | Output voltage, high (BSDA, BSCL) | $I_{\text{OH}} = -1\text{ mA}$ | $V_{\text{CC}} - 0.5$ | | | V |
| $V_{\text{OH(OD)}}$ | Output voltage, high (SDA, SCL, SOC_INT) | External pullup resistor connected to V_{CC} | $V_{\text{CC}} - 0.5$ | | | |
| V_{IL} | Input voltage, low (SDA, SCL) | | -0.3 | | 0.6 | V |
| | Input voltage, low (BI/TOUT) | BAT INSERT CHECK MODE active | -0.3 | | 0.6 | |
| V_{IH} | Input voltage, high (SDA, SCL) | | 1.2 | | | V |
| | Input voltage, high (BI/TOUT) | BAT INSERT CHECK MODE active | 1.2 | $V_{\text{CC}} + 0.3$ | | |
| $V_{\text{IL(CE)}}$ | Input voltage, low (CE) | $V_{\text{REGIN}} = 2.8$ to 4.5 V | | | 0.8 | V |
| $V_{\text{IH(CE)}}$ | Input voltage, high (CE) | | | 2.65 | | |
| $I_{\text{Ikg}}^{(1)}$ | Input leakage current (I/O pins) | | | | 0.3 | μA |

(1) Specified by design. Not production tested.

POWER-ON RESET

 $T_A = -40^{\circ}\text{C}$ to 85°C , typical values at $T_A = 25^{\circ}\text{C}$ and $V_{\text{REGIN}} = 3.6\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|---|------|------|------|------|
| $V_{\text{IT+}}$ | Positive-going battery voltage input at V_{CC} | 2.05 | 2.15 | 2.20 | V |
| V_{HYS} | Power-on reset hysteresis | 45 | 115 | 185 | mV |

2.5V LDO REGULATOR

 $T_A = -40^{\circ}\text{C}$ to 85°C , $C_{\text{LDO25}} = 1\mu\text{F}$, $V_{\text{REGIN}} = 3.6\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITION | MIN | NOM | MAX | UNIT | |
|--------------------|--|---|-----|-----|------|---|
| V_{REG25} | Regulator output voltage (V_{CC}) | $2.8\text{ V} \leq V_{\text{REGIN}} \leq 4.5\text{ V}$, $I_{\text{OUT}} \leq 16\text{ mA}^{(1)}$ | 2.3 | 2.5 | 2.6 | V |
| | | $2.45\text{ V} \leq V_{\text{REGIN}} < 2.8\text{ V}$ (low battery), $I_{\text{OUT}} \leq 3\text{ mA}$ | 2.3 | | | V |

 (1) LDO output current, I_{OUT} , is the total load current. LDO regulator should be used to power internal fuel gauge only.

INTERNAL CLOCK OSCILLATORS

 $T_A = -40^{\circ}\text{C}$ to 85°C , $2.4\text{ V} < V_{\text{CC}} < 2.6\text{ V}$; typical values at $T_A = 25^{\circ}\text{C}$ and $V_{\text{CC}} = 2.5\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|---------------------------|-----|--------|-----|------|
| f_{OSC} | High Frequency Oscillator | | 8.389 | | MHz |
| f_{LOSC} | Low Frequency Oscillator | | 32.768 | | kHz |

ADC (TEMPERATURE AND CELL MEASUREMENT) CHARACTERISTICS

$T_A = -40^{\circ}\text{C}$ to 85°C , $2.4\text{ V} < V_{CC} < 2.6\text{ V}$; typical values at $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 2.5\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|--|---------------------------------------|-----|-----|------------------------|
| V_{ADC1} | Input voltage range (TS) | $V_{\text{SS}} - 0.125$ | | 2 | V |
| V_{ADC2} | Input voltage range (BAT) | $V_{\text{SS}} - 0.125$ | | 5 | V |
| $V_{\text{IN(ADC)}}$ | Input voltage range | 0.05 | | 1 | V |
| G_{TEMP} | Internal temperature sensor voltage gain | | -2 | | mV/ $^{\circ}\text{C}$ |
| $t_{\text{ADC_CONV}}$ | Conversion time | | | 125 | ms |
| | Resolution | 14 | | 15 | bits |
| $V_{\text{OS(ADC)}}$ | Input offset | | 1 | | mV |
| $Z_{\text{ADC1}}^{(1)}$ | Effective input resistance (TS) | 8 | | | M Ω |
| $Z_{\text{ADC2}}^{(1)}$ | Effective input resistance (BAT) | bq27531-G1 not measuring cell voltage | | 8 | M Ω |
| | | bq27531-G1 measuring cell voltage | | 100 | k Ω |
| $I_{\text{lkq(ADC)}}^{(1)}$ | Input leakage current | | | 0.3 | μA |

(1) Specified by design. Not tested in production.

INTEGRATING ADC (COULOMB COUNTER) CHARACTERISTICS

$T_A = -40^{\circ}\text{C}$ to 85°C , $2.4\text{ V} < V_{CC} < 2.6\text{ V}$; typical values at $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 2.5\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|--|---|-------------|-------------|---------------|
| V_{SR} | Input voltage range, $V_{\text{(SRP)}}$ and $V_{\text{(SRN)}}$ | $V_{\text{SR}} = V_{\text{(SRP)}} - V_{\text{(SRN)}}$ | -0.125 | 0.125 | V |
| $t_{\text{SR_CONV}}$ | Conversion time | Single conversion | | 1 | s |
| | Resolution | 14 | | 15 | bits |
| $V_{\text{OS(SR)}}$ | Input offset | | 10 | | μV |
| INL | Integral nonlinearity error | | ± 0.007 | ± 0.034 | % FSR |
| $Z_{\text{IN(SR)}}^{(1)}$ | Effective input resistance | 2.5 | | | M Ω |
| $I_{\text{lkq(SR)}}^{(1)}$ | Input leakage current | | | 0.3 | μA |

(1) Specified by design. Not tested in production.

DATA FLASH MEMORY CHARACTERISTICS

$T_A = -40^{\circ}\text{C}$ to 85°C , $2.4\text{ V} < V_{CC} < 2.6\text{ V}$; typical values at $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 2.5\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|---|--------|-----|-----|--------|
| $t_{DR}^{(1)}$ | Data retention | 10 | | | Years |
| | Flash-programming write cycles ⁽¹⁾ | 20,000 | | | Cycles |
| $t_{WORDPROG}^{(1)}$ | Word programming time | | | 2 | ms |
| $I_{CCPROG}^{(1)}$ | Flash-write supply current | | 5 | 10 | mA |
| $t_{DFERASE}^{(1)}$ | Data flash master erase time | 200 | | | ms |
| $t_{IFERASE}^{(1)}$ | Instruction flash master erase time | 200 | | | ms |
| $t_{PGERASE}^{(1)}$ | Flash page erase time | 20 | | | ms |

(1) Specified by design. Not production tested

I²C-COMPATIBLE INTERFACE COMMUNICATION TIMING CHARACTERISTICS

$T_A = -40^{\circ}\text{C}$ to 85°C , $2.4\text{ V} < V_{CC} < 2.6\text{ V}$; typical values at $T_A = 25^{\circ}\text{C}$ and $V_{CC} = 2.5\text{ V}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|--------------------------------------|-----|-----|-----|---------------|
| t_r | SCL/SDA rise time | | | 300 | ns |
| t_f | SCL/SDA fall time | | | 300 | ns |
| $t_{w(H)}$ | SCL pulse duration (high) | 600 | | | ns |
| $t_{w(L)}$ | SCL pulse duration (low) | 1.3 | | | μs |
| $t_{su(STA)}$ | Setup for repeated start | 600 | | | ns |
| $t_{d(STA)}$ | Start to first falling edge of SCL | 600 | | | ns |
| $t_{su(DAT)}$ | Data setup time | 100 | | | ns |
| $t_{h(DAT)}$ | Data hold time | 0 | | | ns |
| $t_{su(STOP)}$ | Setup time for stop | 600 | | | ns |
| $t_{(BUF)}$ | Bus free time between stop and start | 66 | | | μs |
| f_{SCL} | Clock frequency ⁽¹⁾ | | | 400 | kHz |

(1) If the clock frequency (f_{SCL}) is $> 100\text{ kHz}$, use 1-byte write commands for proper operation. All other transactions types are supported at 400 kHz. (Refer to [I²C INTERFACE](#) and [I²C Command Waiting Time](#))

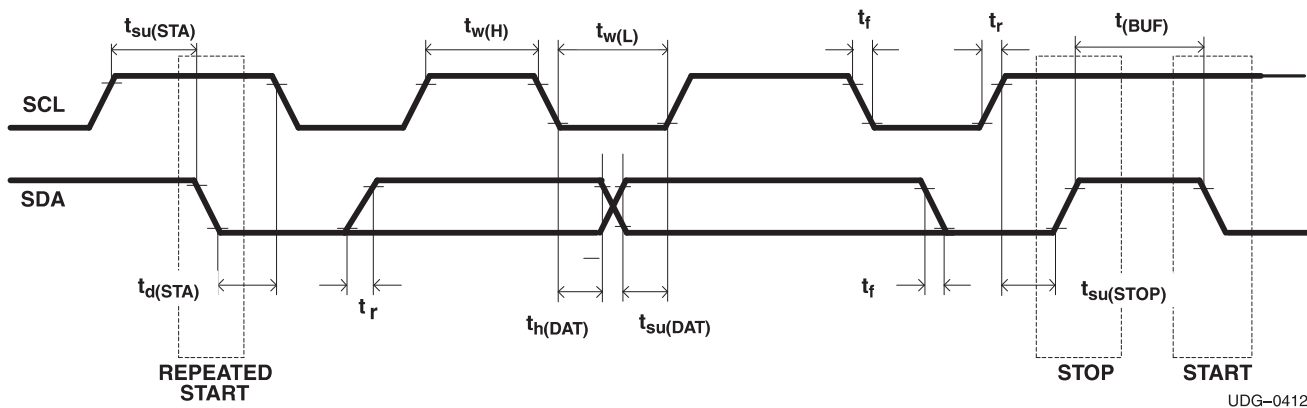


Figure 1. I²C-Compatible Interface Timing Diagrams

GENERAL DESCRIPTION

The bq27531-G1 accurately predicts the battery capacity and other operational characteristics of a single Li-based rechargeable cell. It can be interrogated by a system processor to provide cell information, such as time-to-empty (TTE), and state-of-charge (SOC) as well as SOC interrupt signal to the host.

The bq27531-G1 can control a bq2419x Charger IC without the intervention from an application system processor. Using the bq27531-G1 and bq2419x chipset, batteries can be charged with the typical constant-current, constant voltage (CCCV) profile or charged using a Multi-Level Charging (MLC) algorithm.

Information is accessed through a series of commands, called *Standard Commands*. Further capabilities are provided by the additional *Extended Commands* set. Both sets of commands, indicated by the general format *Command()*, are used to read and write information contained within the device control and status registers, as well as its data flash locations. Commands are sent from system to gauge using the bq27531-G1's I²C serial communications engine, and can be executed during application development, pack manufacture, or end-equipment operation.

Cell information is stored in the device in non-volatile flash memory. Many of these data flash locations are accessible during application development. They cannot, generally, be accessed directly during end-equipment operation. Access to these locations is achieved by either use of the bq27531-G1's companion evaluation software, through individual commands, or through a sequence of data-flash-access commands. To access a desired data flash location, the correct data flash subclass and offset must be known.

The key to the bq27531-G1 high-accuracy gas gauging prediction is Texas Instrument's proprietary Impedance Track™ algorithm. This algorithm uses cell measurements, characteristics, and properties to create state-of-charge predictions that can achieve less than 1% error across a wide variety of operating conditions and over the lifetime of the battery.

The device measures battery charge/discharge activity by monitoring the voltage across a small-value series sense resistor (5 mΩ to 20 mΩ typ.) located between the system's V_{SS} and the battery's PACK- terminal. When a cell is attached to the device, cell impedance is computed, based on cell current, cell open-circuit voltage (OCV), and cell voltage under loading conditions.

The device external temperature sensing is optimized with the use of a high accuracy negative temperature coefficient (NTC) thermistor with R₂₅ = 10.0kΩ ±1%, B_{25/85} = 3435K ± 1% (such as Semitec NTC 103AT). The bq27531-G1 can also be configured to use its internal temperature sensor. When an external thermistor is used, a 18.2k pull up resistor between BI/TOUT and TS pins is also required. The bq27531-G1 uses temperature to monitor the battery-pack environment, which is used for fuel gauging and cell protection functionality.

To minimize power consumption, the device has different power modes: NORMAL, SLEEP, SLEEP+, HIBERNATE, and BAT INSERT CHECK. The bq27531-G1 passes automatically between these modes, depending upon the occurrence of specific events, though a system processor can initiate some of these modes directly.

For complete operational details, refer to [bq27531-G1 Technical Reference Manual](#).

NOTE

FORMATTING CONVENTIONS IN THIS DOCUMENT:

Commands: *italics* with parentheses and no breaking spaces, e.g., *RemainingCapacity()*

Data flash: *italics*, **bold**, and *breaking spaces*, e.g., ***Design Capacity***

Register bits and flags: brackets and *italics*, e.g., [*TDA*]

Data flash bits: brackets, *italics* and **bold**, e.g., [***LED1***]

Modes and states: ALL CAPITALS, e.g., UNSEALED mode.

DATA COMMANDS

STANDARD DATA COMMANDS

The bq27531-G1 uses a series of 2-byte standard commands to enable system reading and writing of battery information. Each standard command has an associated command-code pair, as indicated in [Table 2](#). Because each command consists of two bytes of data, two consecutive I²C transmissions must be executed both to initiate the command function, and to read or write the corresponding two bytes of data. Additional details are found in the [bq27531-G1 Technical Reference Manual](#).

Table 2. Standard Commands

| NAME | COMMAND CODE | UNITS | SEALED ACCESS | UNSEALED ACCESS |
|---------------------------------------|--------------|----------|------------------|------------------|
| <i>Control()</i> | 0x00 / 0x01 | N/A | R/W | R/W |
| <i>AtRate()</i> | 0x02 / 0x03 | mA | R/W | R/W |
| <i>AtRateTimeToEmpty()</i> | 0x04 / 0x05 | Minutes | R | R/W |
| <i>Temperature()</i> | 0x06 / 0x07 | 0.1 K | R/W | R/W |
| <i>Voltage()</i> | 0x08 / 0x09 | mV | R | R/W |
| <i>Flags()</i> | 0x0a / 0x0b | N/A | R | R/W |
| <i>NominalAvailableCapacity()</i> | 0x0c / 0x0d | mAh | R | R/W |
| <i>FullAvailableCapacity()</i> | 0x0e / 0x0f | mAh | R | R/W |
| <i>RemainingCapacity()</i> | 0x10 / 0x11 | mAh | R | R/W |
| <i>FullChargeCapacity()</i> | 0x12 / 0x13 | mAh | R | R/W |
| <i>AverageCurrent()</i> | 0x14 / 0x15 | mA | R | R/W |
| <i>TimeToEmpty()</i> | 0x16 / 0x17 | Minutes | R | R/W |
| <i>RemainingCapacityUnfiltered()</i> | 0x18 / 0x19 | mAh | R | R/W |
| <i>StandbyCurrent()</i> | 0x1a / 0x1b | mA | R | R/W |
| <i>RemainingCapacityFiltered()</i> | 0x1c / 0x1d | mAh | R | R/W |
| <i>ProgChargingCurrent()</i> | 0x1e / 0x1f | mA | R ⁽¹⁾ | R ⁽¹⁾ |
| <i>ProgChargingVoltage()</i> | 0x20 / 0x21 | mV | R ⁽¹⁾ | R ⁽¹⁾ |
| <i>FullChargeCapacityUnfiltered()</i> | 0x22 / 0x23 | mAh | R | R/W |
| <i>AveragePower()</i> | 0x24 / 0x25 | mW | R | R/W |
| <i>FullChargeCapacityFiltered()</i> | 0x26 / 0x27 | mAh | R | R/W |
| <i>StateOfHealth()</i> | 0x28 / 0x29 | % / num | R | R/W |
| <i>CycleCount()</i> | 0x2a / 0x2b | Counters | R | R/W |
| <i>StateOfCharge()</i> | 0x2c / 0x2d | % | R | R/W |
| <i>TrueSOC()</i> | 0x2e / 0x2f | % | R | R/W |
| <i>InstantaneousCurrentReading()</i> | 0x30 / 0x31 | mA | R | R/W |
| <i>InternalTemperature()</i> | 0x32 / 0x33 | 0.1 K | R | R/W |
| <i>ChargingLevel()</i> | 0x34 / 0x35 | HEX | R | R |
| <i>LevelTaperCurrent()</i> | 0x6e / 0x6f | mA | R | R |
| <i>CalcChargingCurrent()</i> | 0x70 / 0x71 | mA | R | R |
| <i>CalcChargingVoltage()</i> | 0x72 / 0x73 | V | R | R |

(1) Only writeable when **Charger Options [BYPASS]** is set.

Control(): 0x00/0x01

Issuing a *Control()* command requires a subsequent 2-byte subcommand. These additional bytes specify the particular control function desired. The *Control()* command allows the system to control specific features of the bq27531-G1 during normal operation and additional features when the device is in different access modes, as described in [Table 3](#). Additional details are found in the [bq27531-G1 Technical Reference Manual](#).

Table 3. Control() Subcommands

| CNTL FUNCTION | CNTL DATA | SEALED ACCESS | DESCRIPTION |
|--------------------|-----------|---------------|---|
| CONTROL_STATUS | 0x0000 | Yes | Reports the status of hibernate, IT, etc. |
| DEVICE_TYPE | 0x0001 | Yes | Reports the device type (eg: 0x0531 for bq27531) |
| FW_VERSION | 0x0002 | Yes | Reports the firmware version on the device type |
| HW_VERSION | 0x0003 | Yes | Reports the hardware version of the device type |
| PREV_MACWRITE | 0x0007 | Yes | Returns previous MAC subcommand code |
| CHEM_ID | 0x0008 | Yes | Reports the chemical identifier of the Impedance Track™ configuration |
| BOARD_OFFSET | 0x0009 | No | Forces the device to measure and store the board offset |
| CC_OFFSET | 0x000a | No | Forces the device to measure the internal CC offset |
| CC_OFFSET_SAVE | 0x000b | No | Forces the device to store the internal CC offset |
| OCV_CMD | 0x000c | Yes | Request the gauge to take a OCV measurement |
| BAT_INSERT | 0x000d | Yes | Forces the BAT_DET bit set when the [BIE] bit is 0 |
| BAT_REMOVE | 0x000e | Yes | Forces the BAT_DET bit clear when the [BIE] bit is 0 |
| SET_HIBERNATE | 0x0011 | Yes | Forces CONTROL_STATUS [HIBERNATE] to 1 |
| CLEAR_HIBERNATE | 0x0012 | Yes | Forces CONTROL_STATUS [HIBERNATE] to 0 |
| SET_SLEEP+ | 0x0013 | Yes | Forces CONTROL_STATUS [SNOOZE] to 1 |
| CLEAR_SLEEP+ | 0x0014 | Yes | Forces CONTROL_STATUS [SNOOZE] to 0 |
| OTG_ENABLE | 0x0015 | Yes | Commands the bq2419x into USB On The Go mode |
| OTG_DISABLE | 0x0016 | Yes | Disables OTG mode at the bq2419x |
| DIV_CUR_ENABLE | 0x0017 | Yes | Makes the programmed charge current to be half of what is calculated by the gauge charging algorithm. |
| CHG_ENABLE | 0x001A | Yes | Enable charger. Charge will continue as dictated by gauge charging algorithm. |
| CHG_DISABLE | 0x001B | Yes | Disable charger (Set \overline{CE} bit of bq2419x) |
| GG_CHGRCTL_ENABLE | 0x001C | Yes | Enables the gas gauge to control the charger while continuously resetting the charger watchdog |
| GG_CHGRCTL_DISABLE | 0x001D | Yes | The gas gauge stops resetting the charger watchdog |
| DIV_CUR_DISABLE | 0x001E | Yes | Makes the programmed charge current to be same as what is calculated by the gauge charging algorithm. |
| DF_VERSION | 0x001F | Yes | Returns the Data Flash Version |
| SEALED | 0x0020 | No | Places device in SEALED access mode |
| IT_ENABLE | 0x0021 | No | Enables the Impedance Track™ algorithm |
| RESET | 0x0041 | No | Forces a full reset of the bq27531-G1 |
| SHIPMODE_ENABLE | 0x0050 | Yes | Commands the bq2419x to turn off BATFET after a delay time programmed in dataflash so that system load does not draw power from battery |
| SHIPMODE_DISABLE | 0x0051 | Yes | Commands the bq2419x to disregard turning off BATFET before delay time or turns on commands BATFET to turn on if an VBUS had power during the SHIPMODE enabling process |

CHARGER DATA COMMANDS

The charger registers are mapped to a series of single byte Charger Data Commands to enable system reading and writing of battery charger registers. During charger power up, the registers are initialized to Charger Reset State. The fuel gauge can change the values of these registers during the System Reset State.

Each of the bits in the Charger Data Commands can be read/write. It is important to note that System Access can be different from the read/write access as defined in bq2419x charger hardware. The fuel gauge may block write access to the charger hardware when the bit function is controlled by the fuel gauge exclusively. For example, the [VREGx] bits of *Chrgr_Voltage_Reg4* are controlled by the fuel gauge and cannot be modified by system.

The bq27531 reads the corresponding registers of *System_Stat_Reg8()* and *Fault_Reg9()* every second to mirror the charger status. Other registers in the bq2419x are read when registers are modified by the bq27531.

Table 4. Charger Data Commands

| NAME | | COMMAND CODE | bq2419x Charger Memory Location | SEALED ACCESS | UNSEALED ACCESS | Refresh Rate |
|---------------------------------|----------|--------------|--|------------------|--------------------|--------------|
| <i>ChargerStatus()</i> | CHGRSTAT | 0x74 | NA | R | R | Every second |
| <i>Chrgr_InCtrl_Reg0()</i> | CHGR0 | 0x75 | 0x00 | R/W | R/W | Data Change |
| <i>Chrgr_POR_Config_Reg1()</i> | CHGR1 | 0x76 | 0x01 | R/W | R/W | Data Change |
| <i>Chrgr_Current_Reg2()</i> | CHGR2 | 0x77 | 0x02 | R/W | R/W | Data Change |
| <i>Chrgr_PreTerm_Reg3()</i> | CHGR3 | 0x78 | 0x03 | R/W | R/W | Data Change |
| <i>Chrgr_Voltage_Reg4()</i> | CHGR4 | 0x79 | 0x04 | R/W | R/W | Data Change |
| <i>Chrgr_TermTimer_Reg5()</i> | CHGR5 | 0x7a | 0x05 | R/W | R/W | Data Change |
| <i>Chrgr_IRThermal_Reg6()</i> | CHGR6 | 0x7b | 0x06 | R/W | R/W | Data Change |
| <i>Chrgr_OpCtrl_Reg7()</i> | CHGR7 | 0x7c | 0x07 | R/W | R/W | Data Change |
| <i>Chrgr_Status_Reg8()</i> | CHGR8 | 0x7d | 0x08 | R/W | R/W | Every Second |
| <i>Chrgr_Fault_Reg9()</i> | CHGR9 | 0x7e | 0x09 | R/W | R/W | Every Second |
| <i>Chrgr_Rev_RegA()</i> | CHGRA | 0x7f | 0x0a | R/W | R/W | Data Change |

FUNCTIONAL DESCRIPTION

The bq27531-G1 measures the cell voltage, temperature, and current to determine battery SOC. The bq27531-G1 monitors charge and discharge activity by sensing the voltage across a small-value resistor (5 mΩ to 20 mΩ typ.) between the SRP and SRN pins and in series with the cell. By integrating charge passing through the battery, the battery's SOC is adjusted during battery charge or discharge.

The total battery capacity is found by comparing states of charge before and after applying the load with the amount of charge passed. When an application load is applied, the impedance of the cell is measured by comparing the OCV obtained from a predefined function for present SOC with the measured voltage under load. Measurements of OCV and charge integration determine chemical state of charge and chemical capacity (Qmax). The initial Qmax values are taken from a cell manufacturers' data sheet multiplied by the number of parallel cells. It is also used for the value in **Design Capacity**. The bq27531-G1 acquires and updates the battery-impedance profile during normal battery usage. It uses this profile, along with SOC and the Qmax value, to determine *FullChargeCapacity*() and *StateOfCharge*(), specifically for the present load and temperature. *FullChargeCapacity*() is reported as capacity available from a fully charged battery under the present load and temperature until *Voltage*() reaches the **Terminate Voltage**. *NominalAvailableCapacity*() and *FullAvailableCapacity*() are the uncompensated (no or light load) versions of *RemainingCapacity*() and *FullChargeCapacity*() respectively.

The bq27531-G1 has two flags accessed by the *Flags*() function that warns when the battery's SOC has fallen to critical levels. When *RemainingCapacity*() falls below the first capacity threshold, specified in **SOC1 Set Threshold**, the [SOC1] (*State of Charge Initial*) flag is set. The flag is cleared once *RemainingCapacity*() rises above **SOC1 Clear Threshold**.

When *Voltage*() falls below the system shut down threshold voltage, **SysDown Set Volt Threshold**, the [SYSDOWN] flag is set, serving as a final warning to shut down the system. The SOC_INT also signals. When *Voltage*() rises above **SysDown Clear Voltage** and the [SYSDOWN] flag has already been set, the [SYSDOWN] flag is cleared. The SOC_INT also signals such change. All units are in mV.

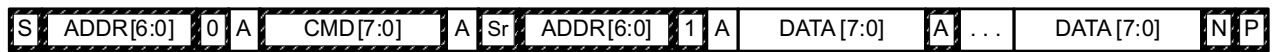
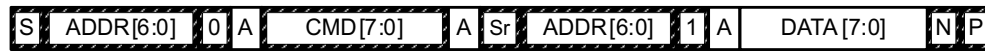
When the voltage is discharged to **Terminate Voltage**, the SOC will be set as 0.

COMMUNICATIONS

I²C INTERFACE

The bq27531-G1 supports the standard I²C read, incremental read, quick read, one-byte write, and incremental write functions. The 7-bit device address (ADDR) is the most significant 7 bits of the hex address and is fixed as 1010101. The first 8 bits of the I²C protocol are, therefore, 0xAA or 0xAB for write or read, respectively.

Host generated Gauge generated

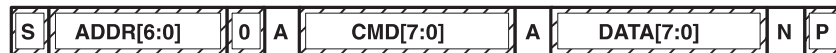


(S = Start, Sr = Repeated Start, A = Acknowledge, N = No Acknowledge, and P = Stop).

The quick read returns data at the address indicated by the address pointer. The address pointer, a register internal to the I²C communication engine, increments whenever data is acknowledged by the bq27531-G1 or the I²C master. "Quick writes" function in the same manner and are a convenient means of sending multiple bytes to consecutive command locations (such as two-byte commands that require two bytes of data).

The following command sequences are not supported:

Attempt to write a read-only address (NACK after data sent by master):



Attempt to read an address above 0x6B (NACK command):

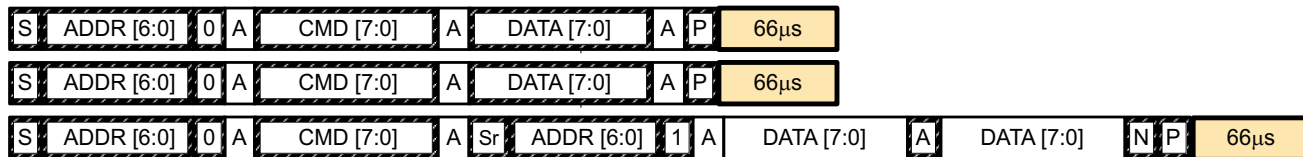


I²C Time Out

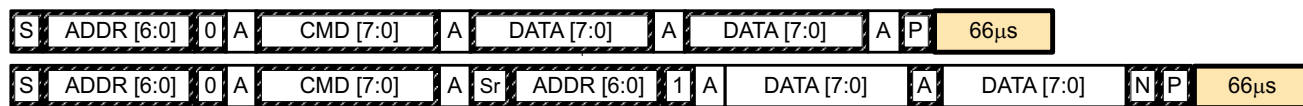
The I²C engine releases both SDA and SCL if the I²C bus is held low for 2 seconds. If the bq27531-G1 is holding the lines, releasing them frees them for the master to drive the lines. If an external condition is holding either of the lines low, the I²C engine enters the low-power sleep mode.

I²C Command Waiting Time

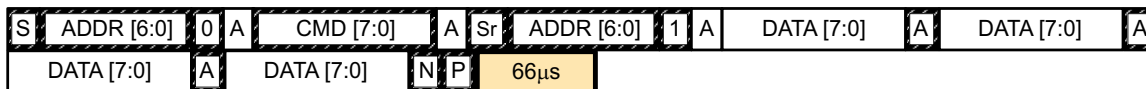
To ensure proper operation at 400 kHz, a $t_{(BUF)} \geq 66 \mu s$ bus-free waiting time must be inserted between all packets addressed to the bq27531-G1. In addition, if the SCL clock frequency (f_{SCL}) is > 100 kHz, use individual 1-byte write commands for proper data flow control. The following diagram shows the standard waiting time required between issuing the control subcommand and the reading the status result. For read-write standard command, a minimum of 2 seconds is required to get the result updated. For read-only standard commands, there is no waiting time required, but the host must not issue any standard command more than two times per second. Otherwise, the gauge could result in a reset issue due to the expiration of the watchdog timer.



Waiting time inserted between two 1-byte write packets for a subcommand and reading results
(required for $100 \text{ kHz} < f_{SCL} \leq 400 \text{ kHz}$)



Waiting time inserted between incremental 2-byte write packet for a subcommand and reading results
(acceptable for $f_{SCL} \leq 100 \text{ kHz}$)



Waiting time inserted after incremental read

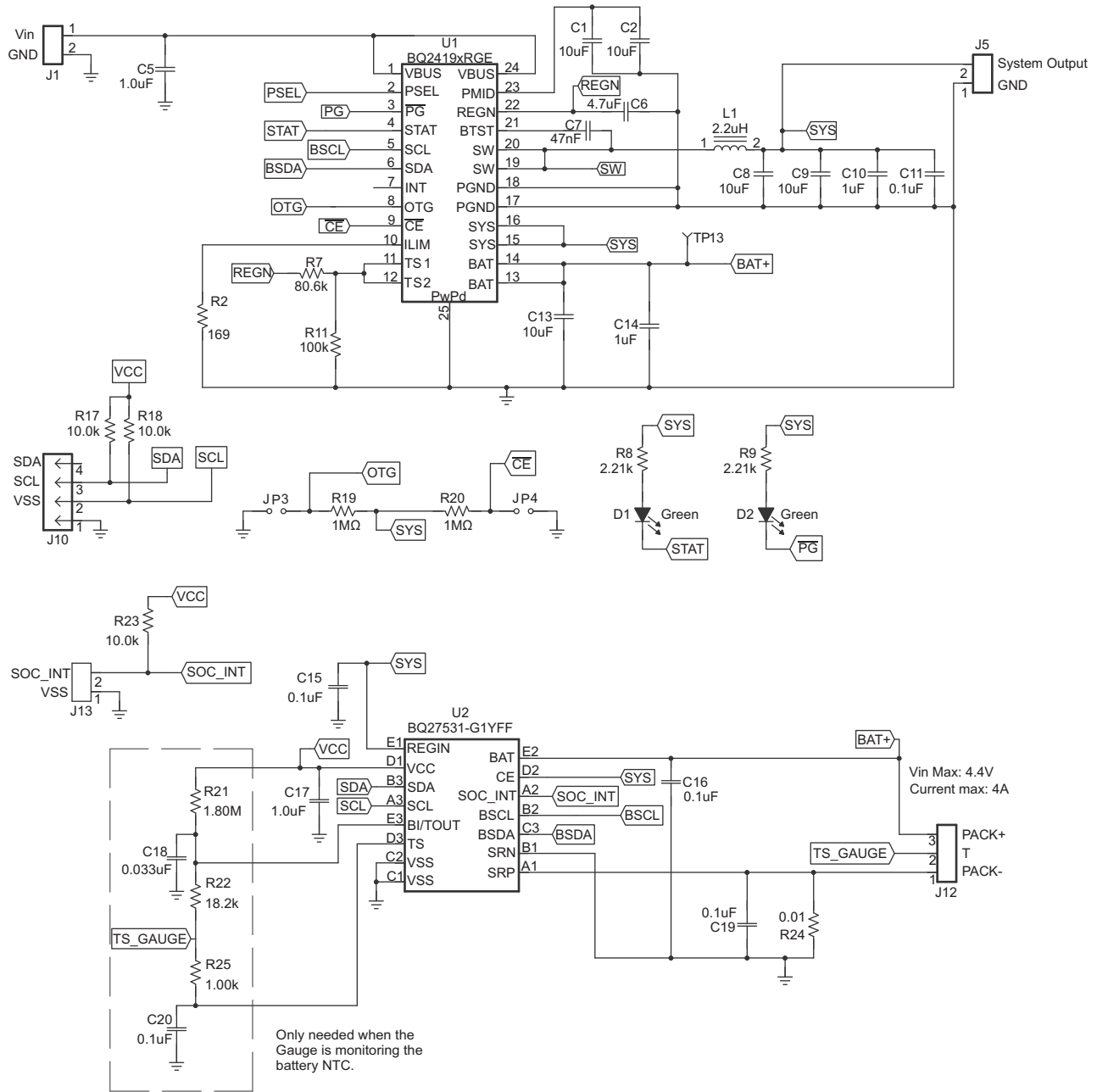
I²C Clock Stretching

A clock stretch can occur during all modes of fuel gauge operation. In SLEEP and HIBERNATE modes, a short clock stretch occurs on all I²C traffic as the device must wake-up to process the packet. In the other modes (BAT INSERT CHECK, NORMAL, SLEEP+) clock stretching only occurs for packets addressed for the fuel gauge. The majority of clock stretch periods are small as the I²C interface performs normal data flow control. However, less frequent yet more significant clock stretch periods may occur as blocks of Data Flash are updated. The following table summarizes the approximate clock stretch duration for various fuel gauge operating conditions.

| Gauging Mode | Operating Condition / Comment | Approximate Duration |
|---|---|----------------------|
| SLEEP HIBERNATE | Clock stretch occurs at the beginning of all traffic as the device wakes up. | $\leq 4 \text{ ms}$ |
| BAT INSERT CHECK NORMAL SLEEP+ | Clock stretch occurs within the packet for flow control (after a start bit, ACK or first data bit). | $\leq 4 \text{ ms}$ |
| | Normal Ra table Data Flash updates. | 24 ms |
| | Data Flash block writes. | 72 ms |
| | Restored Data Flash block write after loss of power. | 116 ms |
| | End of discharge Ra table Data Flash update. | 144 ms |

REFERENCE SCHEMATICS

SCHEMATIC



PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|------------------|---------------|--------------|--------------------|------|-------------|----------------------------|------------------|----------------------|--------------|--------------------------|---------|
| BQ27531YZFR-G1 | PREVIEW | DSBGA | YZF | 15 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | BQ27531 | |
| BQ27531YZFT-G1 | PREVIEW | DSBGA | YZF | 15 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | BQ27531 | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

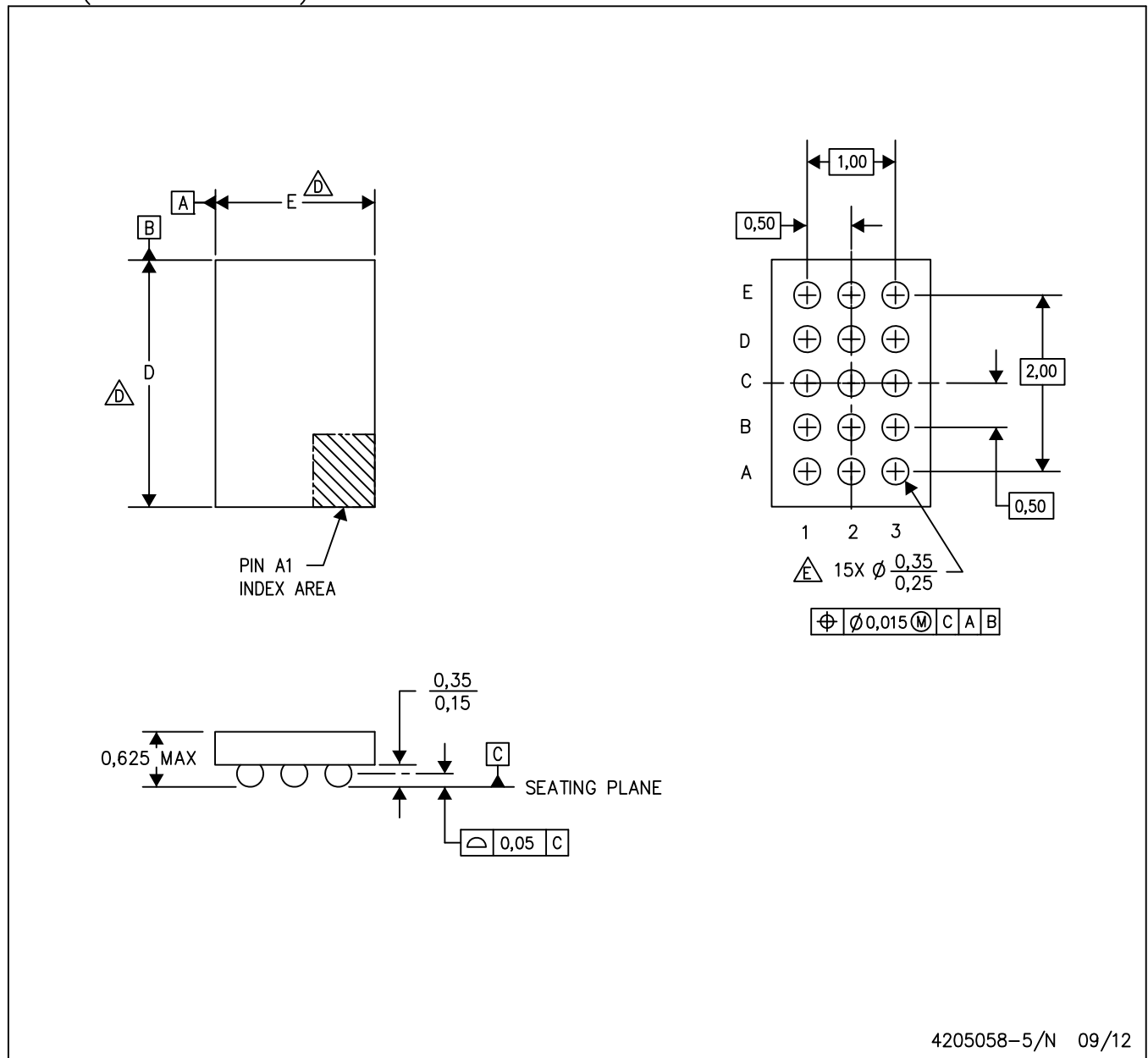
(4) Only one of markings shown within the brackets will appear on the physical device.

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YZF (R-XBGA-N15)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - $\triangle D$ The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
 - $\triangle E$ Reference Product Data Sheet for array population.
3 x 5 matrix pattern is shown for illustration only.
 - F. This package contains Pb-free balls.

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